Reconfigurable Data Path Processor

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***Abstract* – The Reconfigurable Data Path Processor is a multi-processing integrated circuit under development for data intensive, streaming applications aboard spacecraft. It is targeted to an ultra-low-power, radiation-tolerant CMOS technology. In addition to the processor chip, a suite of support software is being developed.**

I. Introduction

The Reconfigurable Data Path Processor (RDPP) is conceived as an ultra-low-power, radiation-tolerant processor for data-intensive, streaming applications such as image and signal processing. Sophisticated space-borne instruments require high-performance data processors. However, the special requirements of space, especially radiation tolerance and low power consumption, impede the use of commercial high-performance processors. High-performance sequential processors, including digital signal processors (DSPs), achieve their performance through complex control strategies and high clock rates. The aggressive circuit design techniques required to support high clock rates consume a significant amount of power, and are not amenable to radiation hardening. When sequential devices are implemented in radiation-tolerant processes, the performance is severely degraded.

The emerging field of Reconfigurable Computing promises to increase throughput at modest clock rates with data-path parallelism, while preserving flexibility through reconfiguration [1]. To date, the bulk of reconfigurable computing research has focused on high-performance, commercial programmable logic devices such as Field Programmable Gate Arrays (FPGAs). FPGA architectures are not always optimal for space applications, however. Their fine granularity exacts a high price in area efficiency: most of the chip is dedicated to interconnects and configuration registers, sometimes leaving as little as one percent of the chip for application logic [2]. Like sequential processors, high-performance FPGAs are power-hungry and difficult to manufacture in radiation-tolerant processes.

The Reconfigurable Data Path Processor is designed with a coarser reconfiguration granularity than FPGAs, but is significantly more reconfigurable than sequential processors. The RDPP architecture emphasizes a highly-parallel, configurable data path [3]. The RDPP will serve as an accelerator to a sequential host processor. The principal design goals are:

1. High-throughput, low-power operations on streams of data.
2. Designer-friendly, with good software support.
3. Radiation-tolerant.
4. Adaptable to a wide range of spacecraft instrument applications.

II. RDPP Architecture

The Reconfigurable Data Path Processor embodies sixteen processing elements (PEs). Each processing element is fed by three 24-bit inputs and two 24-bit outputs. Each PE contains a multiplier, a general-purpose Arithmetic-Logic Unit (ALU), data path formatting elements, a conditional multiplexer, and two internal data registers. Programmable interconnects manage the connections between these computational modules within the PE. The PEs are connected to one another by a hierarchical, programmable interconnect network [4].

The RDPP implements a synchronous data flow computational model [5]. In this “non-blocking read, blocking-write” model, processing elements are connected in a computational pipeline which may include parallel branches. A PE begins computation as soon as input data become available. The PE *fires*, and passes computational

results on to successors, when (1) the computation is complete, and (2) the successor PEs are ready to receive new input.

A key element of synchronous data flow is computationally-dependent, conditional data path switching. A sequential processor achieves instruction execution agility through conditional branching. The RDPP run-time model does not support conditional branching; instead, both computations are carried out simultaneously in parallel branches. Where the two branches join, conditional data path switching selects one or the other, but not both, to be passed on down the computational chain. In the RDPP, every processing element can serve as a conditional *join* node.

Fig. 1 illustrates a processing pipeline with five processing elements. The parameter τ indicates the processing delay through each PE. x_k is an input data sample at time k, and y_k is an output sample. The pipeline has two parallel branches; processing element PE4 is the join node.

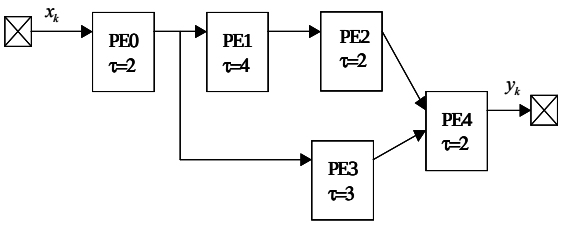

Fig. 1: A processing pipeline.

III. Run-Time Model

The RDPP executes in computational *epochs* consisting of a *configuration phase* followed by an *execution phase* [1]. In configuration, a pipeline is constructed: the individual PEs are configured to perform specific tasks, and the PEs are connected into a network. In execution, a stream of data is clocked through the pipeline in three stages. An *initialization* stage primes the pipe, loading the PEs with data; a steady-state *run* stage processes the data stream; and a *termination* stage empties the pipeline. Then a second epoch begins, in which the PE is reconfigured to form a new pipeline.

Each processing element has only one bit of run-time control, which instructs PE to fire, i.e., to latch its computed data to the output. An on-chip micro-sequencer coordinates the firing of the processing elements.

IV. Implementation Technology

The RDPP is targeted to an ultra-low-power, radiation-tolerant (ULP/RT) CMOS process under development at the Institute of Advanced Microelectronics [6]. Based on a commercial 0.35μ process, the technology employs a minor process variation and back-biasing techniques to operate with a supply voltage of just 0.5V. This significantly reduces the dynamic power consumption, but increases the static consumption [7]. The goal is to balance dynamic and static power consumption to achieve minimum overall power consumption.

Operating in this low-voltage regime has several implications for the RDPP architecture. The power cost of switching is very low (compared to high-voltage CMOS technologies), which encourages highly parallel data path designs and conditional data path switching. Unused processing elements can be shut down by adjusting the back bias to raise the switching threshold to a level that prevents the PE from responding to signals. This also reduces the leakage current, and so throttles static power consumption. Finally, low-voltage design requires special care in modules like memories and crossbars to avoid excessive power loss through leakage.

The ULP/RT technology addresses three aspects of radiation tolerance. The technology achieves single-event latchup (SEL) immunity through layout techniques, and single-event upset (SEU) immunity with a specialized, twelve-transistor memory element [8]. The back biasing technique used to operate at low voltages also raises the thresholds of parasitic field transistors, providing significant total-dose protection.

V. Software Support

In order to achieve its potential in spacecraft instruments, the RDPP must be easy to design with, and must fit into existing instrument design flows. Data processing for space experiments typically begins with the development of signal processing and analysis algorithms, simulated in a workstation-based development environment such as Matlab. Optimized for algorithm design, these environments employ floating point arithmetic, and are not constrained by power consumption, real-time speed, or memory. The instrument designer's challenge is to map an algorithm from unconstrained *simulation space* to highly-constrained, flight-qualified *implementation space*. For the RDPP, this mapping requires several steps:

1. Convert sequential, floating-point algorithms to highly-parallel, fixed-point algorithms.

2. Translate the algorithm to the RDPP programming language, incorporating real-time constraints.

3. Validate and verify the RDPP implementation.

1) *Algorithm Conversion*. The RDPP employs fixed-point arithmetic in order to take advantage of the hardware simplicity, speed, and predictability of fixed-point computation. Converting floating-point software to fixed point while preserving numerical accuracy is a tedious and time-consuming process, typically carried out by trial and error, often yielding sub-optimal results. The RDPP project is developing a set of software tools, called SIFTools, to accelerate this process [9]. The approach is based on a Sign/Integer/Fraction representation of fixed-point numbers, and incorporates a set of formatting rules and policies to assist the designer in building efficient fixed-point data paths that achieve high throughput while preserving accuracy.

2) *Program Translation*. Whereas familiar programming languages such as C++ implement a sequential computational model, the RDPP implements a synchronous data flow model. This model is captured in a variety of design-entry tools, such as Simulink [10], Ptolemy [11], Signal Processing Workstation [12], and Cantata [13]. The RDPP software suite is being developed to facilitate conversion from these dataflow environments to the RDPP programming language. A compiler will complete the translation to RDPP configuration and run-time code.

3) *Validation and Verification*. An RDPP simulator is being developed to enable standalone validation and verification of an implementation before the instrument designer invests in designing and building hardware. The simulator will read the configuration and run-time code produced by the compiler, and perform both functional and timing simulation.

VI. Conclusion

The Reconfigurable Data Path Processor is being developed to integrate emerging technologies into a new processor architecture to enable high-throughput, low-power, radiation-tolerant processing for streaming spacecraft instrument applications. The RDPP combines concepts from Reconfigurable Computing with an ultra-low-power, radiation-tolerant CMOS implementation technology to provide instrument designers with a low-power, space-qualified alternative to high-performance sequential processors or field-programmable gate arrays. A suite of software tools is under development to facilitate integrating the RDPP into spacecraft instruments.

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